Application No.: 10/698,805 Docket No.: MWS-058RCE

REMARKS

In this Response, claims 1, 9, 32 and 42 have been amended. Claims 11-31, 38-41 and 43-44 remain withdrawn. Claims 1-10, 32-37 and 42 are currently pending, of which claims 1, 32 and 42 are independent. No new matter has been added. Support for the amendments to claims 1, 32 and 42 can be found at least in Applicants' specification at page 14, lines 16-18 and page 8, last line – page 9, line 2.

I. Summary of Claim Rejections

The Examiner rejects claim 42 under 35 U.S.C. § 102(e) as being anticipated by United States Patent Number 7,167,817 to Mosterman et al. (hereafter "Mosterman").

The Examiner rejects claims 1, 2, 6, 7, 10, 32, 36, 37 and 42 under 35 U.S.C. § 102(b) as being anticipated by United States Patent Number 6,411,923 to Stewart et al. (hereafter "Stewart").

The Examiner rejects claims 1-7, 9-10, 32-37 and 42 under 35 U.S.C. § 102(b) as being anticipated by United States Patent Number 6,470,482 to Rostoker et al. (hereafter "Rostoker").

The Examiner rejects claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Rostoker as applied to claim 2 in view of "SIMULINK Model-Based and System-Based Design," Version 4, by The MATHWORKS (hereafter "Simulink, Version 4").

II. Claim Rejections under 35 U.S.C. § 102

A. The Mosterman Reference

The Examiner rejects claim 42 under 35 U.S.C. § 102(e) as being anticipated by Mosterman (Office Action, paragraphs 4-5). Applicants respectfully traverse the 35 U.S.C. § 102(e) rejection of claim 42 for at least the reasons set forth below.

Amended independent claim 42 recites:

> "A system for generating and displaying a modeling application for simulating a dynamic system, comprising:
>
> user-operable input means for inputting data to the application;
>
> a display device for displaying an executable graphical model representing the dynamic system; and
>
> an electronic device including memory for storing computer program instructions and data, and a processor for executing the stored computer program instructions, the computer program instructions including instructions for performing a non-virtual operation on a bus signal displayed in the graphical model, wherein the bus signal comprises a first data signal of a first signal type and a second data signal of a second signal type grouped together to form the bus signal, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity."

Mosterman discusses a method and apparatus of resolving artificial algebraic loops, that include providing an executable process having a plurality of functions (Mosterman, abstract). An analysis step identifies whether the process includes at least one potential artificial algebraic loop (Mosterman, abstract). If at least one potential artificial algebraic loop exists in the process, an artificial algebraic loop solution manipulates the order or manner by which the functions are executed to eliminate or otherwise resolve the artificial algebraic loop (Mosterman, abstract).

Applicants respectfully submit that the Mosterman reference fails to disclose every feature of amended independent claim 42. For example, Mosterman does not disclose at least the following feature of amended claim 42: "an electronic device including memory for storing computer program instructions and data, and a processor for executing the stored computer program instructions, the computer program instructions including ***instructions for performing a non-virtual operation on a bus signal displayed in the graphical model***, wherein the bus signal comprises a first data signal of a first signal type and a second data signal of a second signal type grouped together to form the bus signal, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity." [emphasis added]

The Examiner states at paragraph 4 in the Office Action:

> "Applicants persuasively argue that Mosterman does not disclose providing a bundle of signals (bus) as input to a non-virtual operation block.
> However, independent claim 42 has been amended to replace the phrase "performing a non-virtual operation on a bus signal" to the broader language "performing an operation on a bus signal." Both the instant application (page 4) and Mosterman (column 5, lines 10-28) describe the "bus creator" and "bus selector" as performing virtual ***operations*** on a bus signal. Therefore, the Mosterman reference anticipates the invention of claim 42 and Applicants' arguments with respect to that claim are unpersuasive."

The Examiner admits that Mosterman does not disclose providing a bundle of signals as input to a non-virtual operation block (Office Action, paragraph 4). Applicants have amended independent claim 42 to recite "performing a non-virtual operation on a bus signal." Applicants respectfully submit that Mosterman fails to disclose performing a non-virtual operation on a bus signal, as required by claim 42. Mosterman discusses ***a virtual bus creator block and a virtual bus selector block*** for grouping signals into bundles (Mosterman, column 5, lines 10-27). However, Mosterman fails to address performing ***non-virtual operations*** on any type of bus signal or signal bundle, as required by claim 42.

For at least the reasons presented above, Applicants respectfully request reconsideration and allowance of claim 42.

B. The Stewart Reference

The Examiner rejects claims 1, 2, 6, 7, 10, 32, 36, 37 and 42 under 35 U.S.C. § 102(b) as being anticipated by Stewart (Office Action, paragraph 5). Applicants respectfully traverse the 35 U.S.C. § 102(b) rejections of claims 1, 2, 6, 7, 10, 32, 36, 37 and 42 for at least the reasons set forth below.

i) Claim 1

Amended independent claim 1 recites:

> "In an electronic device, a method comprising the steps of:
> grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in an executable graphical model displayed on a graphical user interface, said first signal type specifying a first set

> of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity;
>
> providing the bus signal as input to a non-virtual operation block; and
>
> performing an operation on the bus signal with the non-virtual operation block."

Applicants respectfully submit that the Stewart reference fails to disclose every feature of amended independent claim 1. For example, Stewart does not disclose the following feature of amended claim 1: "***grouping a first data signal of a first signal type and a second data signal of a second signal type*** to form a bus signal in ***an executable graphical model*** displayed on a graphical user interface, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity." [emphasis added]

The Examiner states at paragraph 5 in the Office Action:

> "Regarding claims 1, 2, 6, 7, 10, 32, 36, 37, and 42, Stewart discloses a system, medium, and method for generating and displaying a modeling application for simulating a dynamic system, comprising:
>
> an electronic device including memory for storing computer program instructions and data (FIG. 1, ref 132); (column 4, lines 10-33), and a processor for executing the stored computer program instructions (FIG. 1, ref 134); (column 4, lines 10-33), the computer program instructions including instructions for performing a non-virtual operation on a bus signal displayed in the graphical model, wherein the bus signal comprises first data signal of a first signal type and a second data signal of a second signal type grouped to form a bus signal *["The Fieldbus protocol is an all digital, two-wire loop protocol." (column 2, lines 17-19); (FIG. 6A, 6B, etc.) showing bus segments connecting various "non-virtual" operational blocks, see (column 3, lines 28-42); (column 4, lines 10-33); (column 6, lines 40-67); etc.]*." [emphasis added]

Claims 1 and 32 do not recite "an electronic device including memory for storing computer program instructions and data (FIG. 1, ref 132); (column 4, lines 10-33), and a processor for executing the stored computer program instructions (FIG. 1, ref 134); (column 4, lines 10-33), the computer program instructions including instructions for performing a non-

virtual operation on a bus signal displayed in the graphical model," alleged by the Examiner. A 35 U.S.C. § 102 rejection requires that a single reference disclose all features of a claim. Applicants respectfully point out that the Examiner is mistaken in saying that claim 1 recites "an electronic device including memory for storing computer program instructions and data (FIG. 1, ref 132); (column 4, lines 10-33), and a processor for executing the stored computer program instructions (FIG. 1, ref 134); (column 4, lines 10-33), the computer program instructions including instructions for performing a non-virtual operation on a bus signal displayed in the graphical model," because claim 1 does not include these features.

Stewart fails to disclose an executable graphical model, as required by claim 1. It appears from paragraph 5 of the Office Action that the Examiner is pointing to Figures 6A and 6B in Stewart as disclosing the graphical model recited in claim 1. Applicants respectfully disagree, because Figures 6A and 6B do not disclose an executable graphical model. Figures 6A and 6B are merely screen presentations of the configure segment portion of the topology analysis tool (Stewart, column 3, lines 11-12). A user can configure segment portions by selecting cable length portions, cable type portions, etc, presented on the screen presentations (Stewart, column 6, lines 40-67). The screen presentations in Stewart thus act as ***user interfaces for the configuration of segment portions***. However, Stewart does not disclose that the screen presentations are executable in any way, let alone executable as an executable graphical model as required by claim 1. Therefore, Stewart cannot form the basis of a valid 35 U.S.C. § 102(b) rejection of at least "grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal ***in an executable graphical model*** displayed on a graphical user interface," as required by claim 1.

Stewart fails to disclose still other features of claim 1. For example, Stewart does not disclose "grouping a first data signal of a first signal type and a second data signal of a second signal type, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity," as required by claim 1. Stewart discusses the ***physical characteristics of the wire in the system, e.g. the cable length and cable type***, in connection with the configuration of the segment portions (Stewart, column 6, lines 40-67). However, Stewart does not discuss the ***signal types*** of the data guided by the

Fieldbus protocol in the system. More specifically, Stewart does not disclose data signals of a first signal type and a second signal type, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity. In contrast, claim 1 requires "grouping ***a first data signal of a first signal type*** and ***a second data signal of a second signal type*** to form a bus signal in an executable graphical model displayed on a graphical user interface, ***said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity***."

For at least the reasons presented above, Applicants respectfully request reconsideration and allowance of claim 1.

ii) Claims 2, 6, 7 and 10

Claims 2, 6, 7 and 10 depend from independent claim 1 and, as such, incorporate all of the elements of claim 1. Accordingly, claims 2, 6, 7 and 10 are allowable for at least the reasons set forth above with respect to claim 1. Applicants respectfully request reconsideration and allowance of claims 2, 6, 7 and 10.

iii) Claim 32

Applicants respectfully submit that the arguments set forth above with respect to claim 1 are also applicable to amended claim 32. Accordingly, Applicants respectfully request reconsideration and allowance of claim 32.

iv) Claims 36 and 37

Claims 36 and 37 depend from independent claim 32 and, as such, incorporate all of the elements of claim 32. Accordingly, claims 36 and 37 are allowable for at least the reasons set forth above with respect to claim 32. Applicants therefore respectfully request reconsideration and allowance of claims 36 and 37.

v) Claim 42

Applicants respectfully submit that the Stewart reference fails to disclose every feature of amended independent claim 42. For example, Stewart does not disclose the following features of claim 42: (i) "an executable graphical model," and (ii) "the bus signal comprises a first data signal of a first signal type and a second data signal of a second signal type grouped together to form the bus signal, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity."

As discussed above in connection with claim 1, Stewart fails to disclose: (i) "an executable graphical model," and (ii) "grouping a first data signal of a first signal type and a second data signal of a second signal type, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity." Applicants respectfully submit that the arguments set forth above with respect to claim 1 are also applicable to the features of amended claim 42. Accordingly, Applicants respectfully request reconsideration and allowance of claim 42.

C. The Rostoker Reference

The Examiner rejects claims 1-7, 9-10, 32-37 and 42 under 35 U.S.C. § 102(b) as being anticipated by Rostoker (Office Action, paragraph 6). Applicants respectfully traverse the 35 U.S.C. § 102(b) rejections of claims 1-7, 9-10, 32-37 and 42 for at least the reasons set forth below.

Rostoker discusses a system for interactive design, synthesis and simulation of an electronic system that allows a user to design a system either by specification of a behavioral model in a high level language such as VHDL or by graphical entry (Rostoker, abstract). The user can view full or partial simulation and design results simultaneously, on a single display window (Rostoker, abstract). The simulation results can be displayed immediately adjacent to signal lines on the diagram to which they correspond (Rostoker, abstract).

i) Claim 1

Applicants respectfully submit that the Rostoker reference fails to disclose every feature of amended independent claim 1. For example, Rostoker does not disclose the following feature of amended claim 1: "grouping ***a first data signal of a first signal type*** and ***a second data signal of a second signal type*** to form a bus signal in an executable graphical model displayed on a graphical user interface, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity." [emphasis added]

The Examiner states at paragraph 9 in the Office Action:

> "Regarding claim 1, Rostoker discloses a method comprising the steps of:
> Grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in a graphical model displayed on a graphical user interface ["*A bus signal line 2220 (CTRL<0...3>, representing four physical "wires") connects between the graphical representation 2216 of the microprocessor 2116 and the graphical representation 2214 of the controller 2114 and extends off towards the right hand side of the display screen 2200 (as depicted).*" (column 32, lines 46-51)]; and
> Performing a non-virtual operation on the bus signal [the bus 2220 connects to graphical representation 2214 of the controller 2114, and "The design description 2114a for the other 2114 (CHIP 3) refers to a core cell 2128 (CORE 'C') and a logic block 2130 (misc. logic 'C')." (column 32, lines 31-33)."

Rostoker fails to disclose "grouping ***a first data signal of a first signal type*** and ***a second data signal of a second signal type*** to form a bus signal in an executable graphical model displayed on a graphical user interface, ***said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity***," as recited in claim 1. It appears from the Office Action that the Examiner is pointing to the bus signal line 2220 in the Rostoker reference as disclosing the bus signal recited in Applicants' claim 1. Applicants respectfully disagree, because the disclosure of Rostoker does not indicate that the bus signal line 2220 carries data signals of different signal types, as required by claim 1.

The Examiner relies on column 32, lines 46-51, or Rostoker, for discussing a bus signal line 2220 as four virtual wires connecting the graphical representation of a microprocessor with the graphical representation of a controller. However, Rostoker fails to disclose that the bus signal line 2220 carries data signals of a first signal type and a second signal type, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity, as required by claim 1. Rostoker simply mentions at column 32, lines 53-55 that the bus signal line carries simulation results. Claim 1 describes a signal type as specifying a set of signal attributes that include a data type or a data complexity. Rostoker does not provide any teaching on the data types or the data complexities of the simulation results carried on the bus signal line. Thus, Rostoker cannot disclose that the bus signal line carries data signals of different signal types. In contrast, claim 1 requires "grouping ***a first data signal of a first signal type*** and ***a second data signal of a second signal type*** to form a bus signal in an executable graphical model displayed on a graphical user interface, ***said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity***."

For at least the reasons presented above, Applicants respectfully request reconsideration and allowance of claim 1.

ii) Claims 2-7 and 9-10

Claims 2-7 and 9-10 depend from independent claim 1 and, as such, incorporate all of the elements of claim 1. Accordingly, claims 2-7 and 9-10 are allowable for at least the reasons set forth above with respect to claim 1. Applicants therefore respectfully request reconsideration and allowance of claims 2-7 and 9-10.

iii) Claim 32

Applicants respectfully submit that the arguments set forth above with respect to claim 1 are also applicable to amended claim 32. Accordingly, Applicants respectfully request reconsideration and allowance of claim 32.

iv) Claims 33-37

Claims 33-37 depend from independent claim 32 and, as such, incorporate all of the elements of claim 32. Accordingly, claims 33-37 are allowable for at least the reasons set forth above with respect to claim 32. Applicants therefore respectfully request reconsideration and allowance of claims 33-37.

v) Claim 42

Applicants respectfully submit that the Rostoker reference fails to disclose every feature of amended independent claim 42. For example, Rostoker does not disclose the following features of claim 42: (i) "an executable graphical model," and (ii) "the bus signal comprises a first data signal of a first signal type and a second data signal of a second signal type grouped together to form the bus signal, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity."

As discussed above in connection with claim 1, Rostoker fails to disclose: (i) "an executable graphical model," and (ii) "grouping a first data signal of a first signal type and a second data signal of a second signal type, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity." Applicants respectfully submit that the arguments set forth above with respect to claim 1 are also applicable to the features of amended claim 42. Accordingly, Applicants respectfully request reconsideration and allowance of claim 42.

III. Claim Rejections under 35 U.S.C. § 103

The Examiner rejects claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Rostoker as applied to claim 2 in view of the Simulink, Version 4 reference (Office Action, paragraph 11). Applicants respectfully traverse the 35 U.S.C. § 103(a) rejection of claim 8 for at least the reasons set forth below.

Claim 8 depends from independent claim 1. Therefore, claim 8 includes the features of claim 1. Applicants respectfully submit that Rostoker and Simulink, Version 4, alone or in any reasonable combination, fail to disclose or suggest all of the features of claim 8.

Applicants respectfully submit that Rostoker and Simulink, Version 4 fail to disclose or suggest at least the following feature of claim 8: "grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in an executable graphical model displayed on a graphical user interface, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity."

Rostoker has been summarized above in the rejection of claim 1. As discussed previously, Rostoker fails to disclose or suggest the above feature of claim 8. The teachings of Simulink, Version 4 do not supplement Rostoker in such a way as to cure Rostoker's failure to disclose or suggest the above features of claim 8.

Simulink, Version 4 provides general instructions on the use of SIMULINK for performing model-based and system-based design, and fails to disclose or suggest "grouping a first data signal of a first signal type and a second data signal of a second signal type to form a bus signal in an executable graphical model displayed on a graphical user interface, said first signal type specifying a first set of signal attributes that include a first data type or a first data complexity and said second signal type specifying a second set of signal attributes that include a second data type or a second data complexity." Therefore, Rostoker and Simulink, Version 4, alone or in any reasonable combination, do not support a valid 35 U.S.C. § 103(a) rejection of claim 8. Accordingly, Applicants respectfully request reconsideration and allowance of claim 8.

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CONCLUSION

In view of the above comments, Applicants believe the pending application is in condition for allowance and urge the Examiner to pass the claims to allowance. Should the Examiner feel that a teleconference would expedite the prosecution of this application, the Examiner is urged to contact the Applicants' attorney at (617) 227-7400.

Please charge any shortage or credit any overpayment of fees to our Deposit Account No. 12-0080, under Order No. MWS-058RCE. In the event that a petition for an extension of time is required to be submitted herewith, and the requisite petition does not accompany this response, the undersigned hereby petitions under 37 C.F.R. § 1.136(a) for an extension of time for as many months as are required to render this submission timely. Any fee due is authorized to be charged to the aforementioned Deposit Account.

Dated: November 13, 2007

Respectfully submitted,

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